When building an oscillation circuit with a quartz crystal unit, the following items should be considered.

1. Typical Oscillation Circuit (Fundamental oscillation mode)

A typical oscillation circuit diagram is shown in Fig.7.

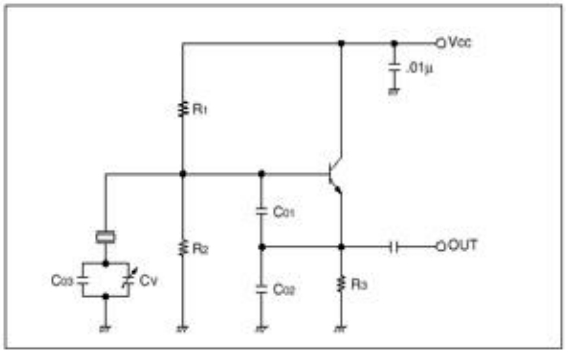


Fig.7 Typical oscillation circuit in fundamental vibration mode

When the oscillation mode is in a steady state, the relations among the reactance of crystal unit Xe, circuit reactance -X, impedance of crystal Re and circuit impedance -R are as follows:

$$Xe = -X$$
$$Re = |-R| \quad \cdots (1)$$

And the simplified oscillation circuit in a steady state is shown in Fig.8.

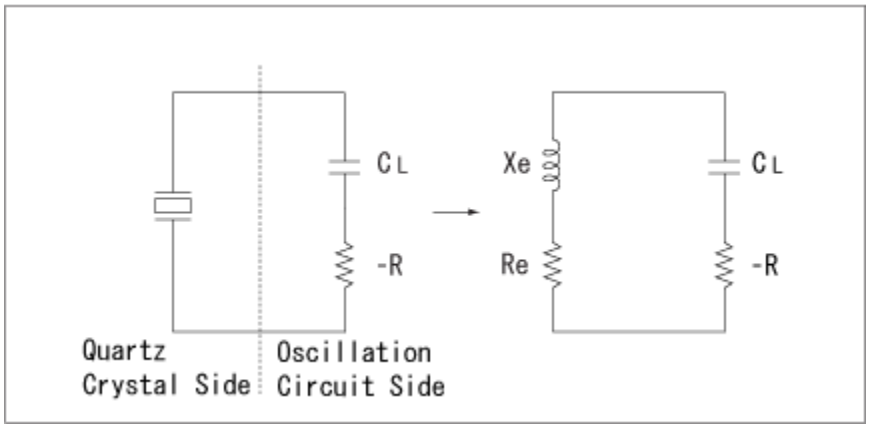


Fig.8 Equivalent oscillation circuit of parallel resonance oscillation circuit

To obtain secure oscillation of the circuit, the negative resistance of the circuit must satisfy the following equation : -R | < Re.

Taking the circuit in Fig.7 as an example, the negative resistance of the circuit is shown as follows:

$$-R = -gm/(\omega^2 \cdot C_{01} \cdot C_{02}) \quad \cdots (2)$$

Here,

gm = Mutual conductance of a transistor at the oscillation stage

$\omega\ (=2\pi \cdot f)$= Oscillation angle frequency

2. Load capacitance and oscillation frequency

Given that

Series resonance frequency = fr

Equivalent Series Capacitance = C1

Parallel Capacitance = C0

Resonance Frequency (With Load Capacitance CL) = fL

and fL - fr = Δf

then,

$$\frac{\Delta f}{f_r} = \frac{f_L - f_r}{f_r} \approx \frac{1}{2(C_0/C_1)} \cdot \frac{1}{1+C_L/C_0} = \frac{C_0}{2\gamma(C_0+C_L)} \quad \cdots (3)$$

The above equation is induced.

The load capacitance can be regarded as the series capacitance of C01,

C02 and C03 + CV, as shown in Fig.7., including stray capacitances oftransistors and circuit patterns.

Therefore, the load capacitance CL is given by the following equation.

$$C_L = \left(\frac{1}{C_{01}} + \frac{1}{C_{02}} + \frac{1}{C_{03}+C_V} \right)^{-1} \quad \cdots (4)$$

The "pulling range", the frequency variation range when the load capacitance of the oscillation circuit can be altered from CL1 to CL2, is expressed as,

$$P.R. = \left| \frac{f_{L1} - f_{L2}}{f_r} \right| = \left| \frac{C_1(C_{L2}-C_{L1})}{2(C_0+C_{L1})(C_0+C_{L2})} \right| \quad \cdots (5)$$

If the equivalent series capacitance C1, parallel capacitance C0, and the above CL1 and CL2 are given, the frequency variation range can be induced from the above equation. The "pulling Sensitivity", the sensitivity of an element near the load capacitance (CL), is given by the following equation.

$$S=\frac{(\Delta f/f_r)}{C_L}\simeq-\frac{C_1}{2(C_0+C_L)^2} \quad \cdots (6)$$

The resonance frequency vs. load capacitance characteristics are shown in Fig. 9. The result of calculating the above equations (3), (5), (6)
under the given conditions of C1 = 16fF, C0 = 3.5pF, CL = 30pF, CL1 = 27pF, and CL2 = 33pF.

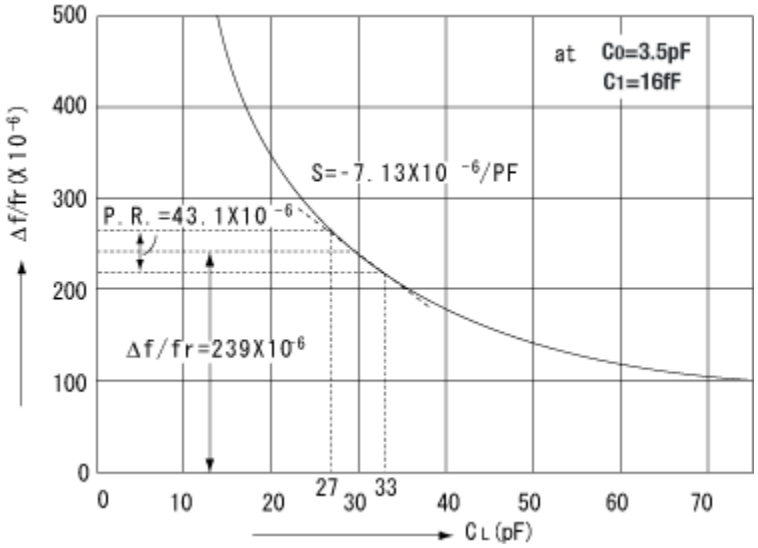


Fig.9 Frequency vs. load capacitance

By applying this phenomenon, the output frequency of the oscillationcircuit can be trimmed to the nominal frequency, by adjusting a variable trimmer capacitor to offset the deviation due to production deviation of the crystal unit and the deviation of components in the oscillation circuit.
Although a reduction in the load capacitance (CL) in Equation (6) will increase the device sensitivity, it will also, conversely, decrease the stability.
Please note that a reduction in the load capacitance will increase the difficulty in starting oscillation because the effective resistance of the crystal unit will increase, as shown in equation (7).

$$R_L=R_1\cdot(1+C_0/C_L)^2 \quad \cdots (7)$$

3. Overtone oscillation circuit

An example of an overtone oscillation circuit is shown in Fig.10. In comparison with a fundamental wave oscillation circuit (Fig.7.), there are two extra inductors in the circuit.

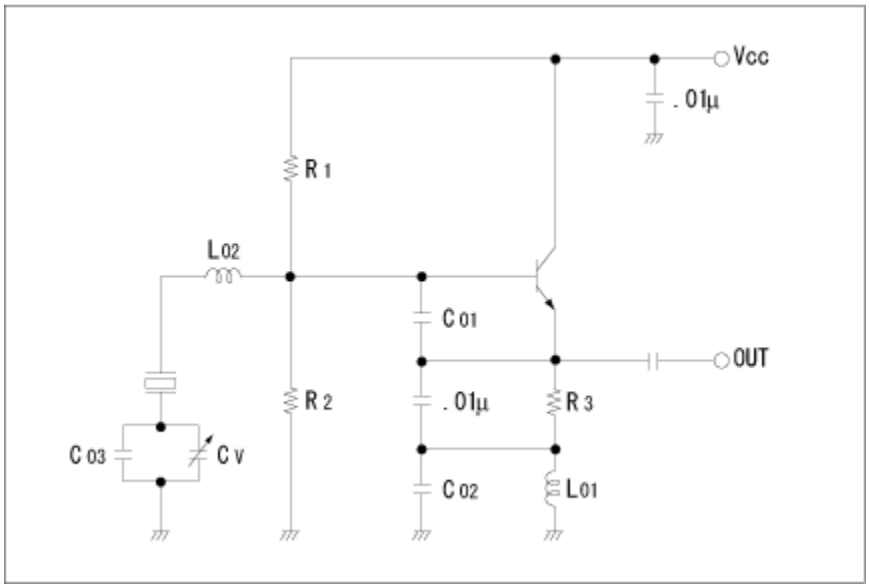


Fig.10 Typical oscillation circuit for overtone frequency

One of the added inductors (L01: Connected to the emitter of a transistor (Q1)) comprises a frequency selection circuit along with C02 connected in parallel, suppressing fundamental or lower oscillation to stabilize overtone oscillation. This loop consisting of L01 and C02 is called a selection circuit. The condition in order to obtain selectivity is the configuration of the values of L01 and C02 so that the parallel resonance frequency of L01 and C02 $f_T(=1/2\pi\sqrt{L_{01}\cdot C_{02}})$ is between the requested overtone frequency and the lower overtone frequency or fundamental frequency.

Next, the negative resistance of this circuit is to be explained further.
In equation (2), if you substitute $(C_{02}-1/\omega^2 L_{01})$ for C02, the negative resistance -R will be $-R=-gm/\{\omega^2\cdot C_{01}\cdot(C_{02}-1/\omega^2\cdot L_{01})\}$.
The negative resistance will reduce in inverse proportion to the square of the frequency. Therefore, C01 and C02 must be of sufficiently small values in the case of overtone oscillation.Another thing to be considered in the case of overtone oscillation is the frequency variable range. In equation (5), the value of the equivalent series capacitance is in inverse proportion to the square of the order of the overtone compared with that of the fundamental oscillation frequency, thus the range of frequency variation will be narrower. Both C01 and C02 will become small to ensure a negative resistance, making frequency tuning more difficult. However, this fact also shows that the

frequency stability against turbulence outside the oscillation loop is heightened. To assure the frequency variable range, an inductor L02 is often added. This inductor, L02, is called an "extension inductor", and the load capacitance and the extension inductor is connected serially, as shown in Fig.11

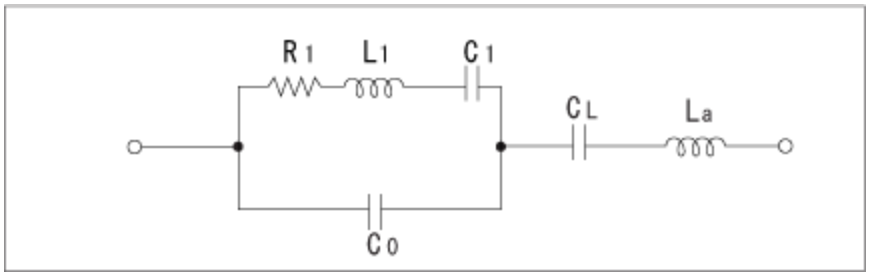


Fig.11 Equivalent circuit with an extension inductor and load capacitance

The variable frequency range at this condition is represented as

$$\frac{\Delta f}{f_r} \simeq \frac{1}{2(C_0/C_1)} \cdot \frac{1}{1+\frac{C_L}{C_0}\cdot\frac{1}{1-\omega^2 L_a C_L}} \quad \cdots (8)$$

In equation (8), if La 0, then equation (3) is induced.
If you add an extensioninductance in this case, please configure the
values of CL and La to satisfy the expression"$1-\omega 2LaCL=0$".
Fig.12 shows a sample oscillation circuit diagram for a pager for your reference.

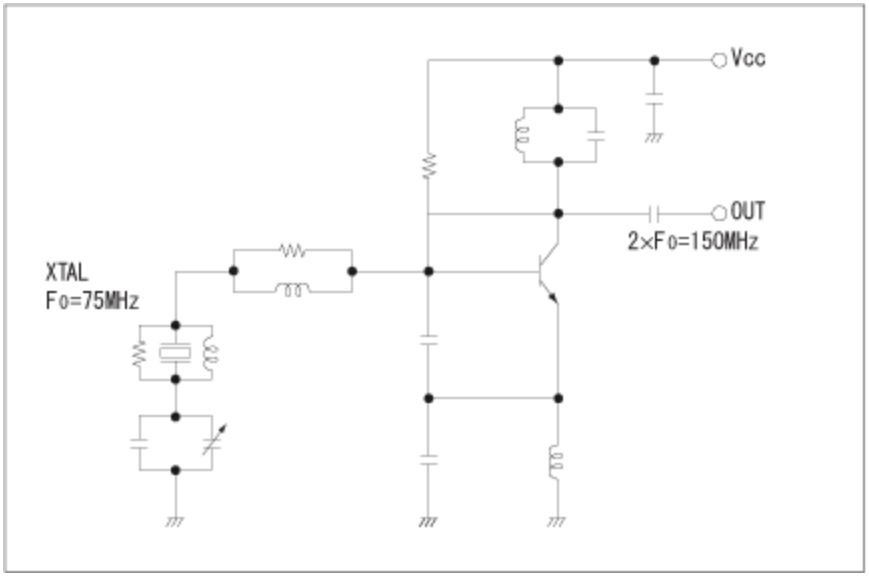
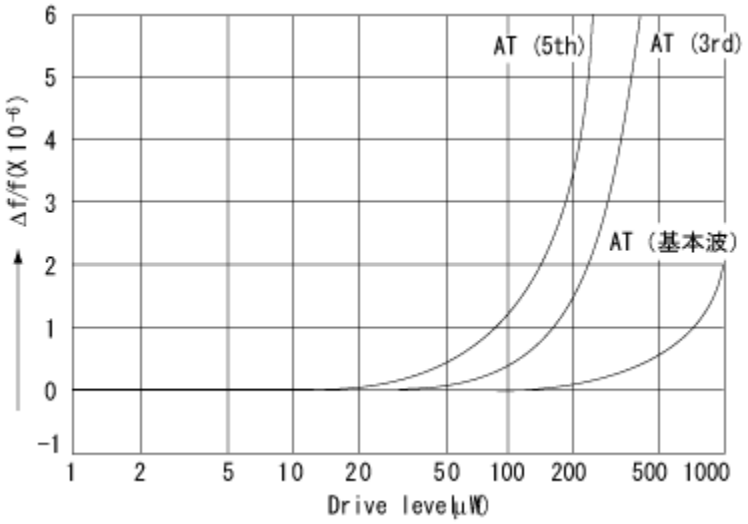


Fig.12 Sample oscillation circuit diagram for a pager for your reference.

4. Drive level of crystal oscillato

In order to ensure the stable oscillation of the crystal oscillator, a certain degree of drive power must be applied. Fig.13 shows how the frequency varies with the drive level, the amount of the frequency shift increasing as the drive level increases.

Applying a high drive power (approx. 50mW) to a crystal unit will cause damage to it. For use in a normal oscillation circuit,
the preferred drive power is 0.1 mW or less (max. 0.5 mW).



5. The following points must be considered when designing a PCB pattern.

The pattern length from the oscillation stage to the crystal unit shall be the minimum in order to keep the stray capacitance of the oscillation loop to a minimum.
When putting other components and wiring patterns over the oscillation loop, the increase of stray capacity shall be kept to a minimum.